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Filing Date	August 24, 2001
First Named Inventor	James M. Derderian
Art Unit	2822
Examiner Name	D. Graybill
Attorney Docket Number	2269-4831US (01-0105.00/US)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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- ☐ CD, Number of CD(s) ____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Brief (19 pages); Claims Appendix (7 pages); Check in the amount of $500.00
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

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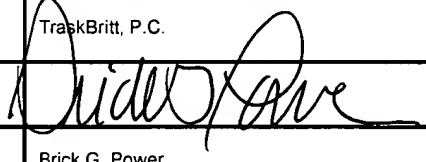
Signature			
Printed Name	Brick G. Power		
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

James M. Derderian

Serial No.: 09/939,258

Filed: August 24, 2001

For: SEMICONDUCTOR DEVICES INCLUDING STACKING SPACERS THEREON, ASSEMBLIES INCLUDING THE SEMICONDUCTOR DEVICES, AND METHODS

Confirmation No.: 2185

Examiner: D. Graybill

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APPEAL BRIEF

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Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

U.S. Application Serial No. 09/939,258 (hereinafter "the '258 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 012121, Frame No. 0051. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellants nor the undersigned attorney are aware of any action pending before the Board of Patent Appeals and Interferences (hereinafter "the Board") that would affect or influence the Board's decision in the above-referenced appeal.

(3) STATUS OF CLAIMS

The '258 Application was filed with fifty-two (52) claims.

Claims 2, 4, 26, 27, and 36-52 have been canceled without prejudice or disclaimer.

Claims 9, 24, 29 have been withdrawn from consideration.

Claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 remain pending and under consideration in the '258 Application.

Claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 are subject to final rejections, which are to be reviewed in the above-referenced appeal.

(4) STATUS OF AMENDMENTS

The '258 Application was filed on August 8, 2001, with fifty-two (52) claims

Claims 1-52 were subject to a Restriction Requirement in a first Office Action mailed September 11, 2003. In an Office Action response mailed September 30, 2003, an election was made, without traverse, to prosecute claims 1-35 of Group I.

On December 30, 2003, an Election of Species Requirement was mailed in a second Office Action. In a response, mailed January 30, 2004, claim 20 was amended, a correction was made to the drawings, and an election was made, without traverse, to prosecute claims 1-8, 10-23, 25-28, and 30-35.

A third Office Action was mailed April 23, 2004. In that Office Action, claim 30 was rejected under both 35 U.S.C. § 112, first paragraph, and 35 U.S.C. § 112, second paragraph. Also, claims 1-8, 10, 12-23, 27, 28, and 30-35 were rejected under 35 U.S.C. § 102(e) for being drawn to subject matter which was allegedly anticipated by the subject matter described in U.S. Patent 6,593,662 to Pu et al. (hereinafter "Pu"). Claims 11, 25 and 26 were rejected under 35 U.S.C. § 103(a) for being directed to subject matter that was assertedly unpatentable over the teachings of Pu, in view of the subject matter taught in U.S. Patent 6,593,662 to Ference et al. (hereinafter "Ference"). A response was filed on July 23, 2004. The response included amendments to claims 1, 3-11, 13-25, and 28-35. Additionally, claims 53 and 54 were added to the application. The response also included explanations as to the patentability of the claims over the numerous rejections that had been presented in the third Office Action.

On October 20, 2004, a fourth Office Action was mailed. In that Office Action, claims 4 and 25 were objected to under 37 C.F.R. § 1.75(c). Claims 18-21, 30, 31, 33-35, and 54 were

rejected under 35 U.S.C. § 102(e) for reciting subject matter which was purportedly anticipated by the subject matter described in U.S. Patent 6,437,449 to Foster (hereinafter "Foster"). Claims 1, 3-8, 10, 12-17, and 53 were rejected under 35 U.S.C. § 103(a) for reciting subject matter which was assertedly unpatentable over that taught in Pu, in view of conventional art, as disclosed in U.S. Publication 2003/0038353 to Derderian (hereinafter "Derderian"). A response to the forth Office Action was filed on January 20, 2005. This response included arguments as to the patentability of the claims over the 35 U.S.C. § 102(e) and 103(a) rejections that had been presented in the fourth Office Action.

On April 22, 2005, a Notice of Non-Responsive Amendment was filed stating that the prior Office Action response was non-responsive for failing to address the objections of claims 4 and 35. A response to the Notice was filed on Monday, May 23, 2005. In the response, claim 4 was canceled without prejudice or disclaimer and an explanation was provided that the Notice of Non-Responsive Amendment had misidentified the objection of claim 35 as an objection to claim 25. Additionally, the response reiterated the arguments as to the patentability of the claims over the 35 U.S.C. § 102(e) and 103(a) rejections that had been presented in the fourth Office Action.

Another Notice of Non-Responsive Amendment was mailed on August 8, 2005, stating that the prior Office Action response was non-responsive for misidentifying claims 1, 3, 5-11, 13-25, and 28-35 as being "Currently amended," with no markings were included to show the amendments to these claims. A response was filed to the Notice of Non-Responsive Amendment which explained that the status identifiers were improper, and replaced the status identifiers with

"Previously presented," as no revisions were made to any of claims 1, 3, 5-11, 13-25, or 28-35 in the Amendment mailed May 23, 2005.

Another Office Action was mailed November 23, 2005. In that Office Action, claims 18-21, 30, 31, 33-35, and 54 were rejected under 35 U.S.C. § 102(e) for reciting subject matter which was purportedly anticipated by that described in Foster. Claims 1, 3, 5-8, 10, 12-17, and 53 were rejected under 35 U.S.C. § 103(a) for reciting subject matter which was assertedly unpatentable over that taught in Pu, in view of teachings from U.S. Patent 6,340,846 to LoBianco, et al. (hereinafter "LoBianco"). Claims 11, 22, 18-23, 25, 28, 30-35 and 54 were rejected under 35 U.S.C. § 103(a) for reciting subject matter which was assertedly unpatentable over that taught in Pu, in view of the subject matter taught in LoBianco and Foster. Finally, claims 1, 3, 5-8, and 10-16 were rejected under 35 U.S.C. § 103(a) for reciting subject matter which was assertedly unpatentable over that taught in Foster, in view of the teachings of LoBianco. In a response to the Office Action of November 23, 2005, explanations were presented as to the patentability of the claims over the numerous rejections that had been presented.

A final Office Action was mailed May 22, 2006. In that Office Action, the Examiner upheld the 35 U.S.C. § 102(e) and 103(a) rejections that had been made in the prior Office Action. In an Amendment Under 37 C.F.R. § 1.116 dated July 27, 2006, Appellants made another attempt to convince the Examiner that the rejected claims are indeed patentable.

The Examiner maintained his final rejections in an Advisory Action dated August 15, 2006.

Accordingly, a Notice of Appeal was filed on August 22, 2006, and is followed within two months by this APPEAL BRIEF, which is being submitted by Monday, October 23, 2006. 37 C.F.R. § 1.7.

(5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Claims 1, 3, 5, 6-17, and 53 of the '258 Application are directed to a semiconductor device assembly. *See, e.g.,* Fig. 1; paragraph **[0040]**. The semiconductor device assembly includes at least one semiconductor device and at least one resiliently compressible spacer protruding from a surface of the at least one semiconductor device, the at least one resiliently compressible spacer defines a distance that the surface of the at least one semiconductor device is to be spaced apart from a surface of another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device. *See, e.g.,* Fig. 1, 10A-10D; paragraphs **[0012]** and **[0046]**.

Claims 18-25, 28-35, and 54 are directed to a semiconductor device assemblythat includes a substrate and a first semiconductor device associated with the substrate. *See, e.g.,* Fig. 1; paragraph **[0040]**. Bond pads of the first semiconductor device communicate with corresponding contact areas of the substrate. *See, e.g.,* Fig. 1; paragraphs **[0041]** and **[0042]**. The semiconductor device also includes mutually laterally spaced discrete spacers positioned on and protruding from an active surface of the first semiconductor device, with at least one spacer being in communication with a ground or reference voltage plane of the first semiconductor device. *See, e.g.,* Fig. 1; paragraphs **[0043]** and **[0044]**. The semiconductor device further includes a second semiconductor device with a back side that is positioned on the mutually

laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane. *See, e.g.,* Fig. 1; paragraphs **[0043]** and **[0045]**.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 102(b) rejections of claims 18-21, 30, 31, 33-35 and 54 for being directed to subject matter which is allegedly anticipated by the subject matter described in Foster;

(B) The rejections of claims 1, 3, 5-8, 10, 12-17, and 53 under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly obvious over the subject matter taught in Pu, in view of teachings from LoBianco;

(C) The rejections of claims 11, 22, 18-23, 25, 28, 30-35, and 54 under 35 U.S.C. § 103(a) for being drawn to subject matter that is assertedly obvious over the subject matter taught in Pu, in view of teachings from LoBianco and, further, in view of the subject matter taught in Foster; and

(D) The rejections of claims 1, 3, 5-8, and 10-16 under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Foster, in view of subject matter taught in LoBianco.

(7) ARGUMENT

(A) REJECTIONS UNDER 35 U.S.C. § 102

(1) LEGAL AUTHORITY

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

(2) ART RELIED UPON

Foster

Foster discloses a packaged multi-chip module assembly. A semiconductor die 108 is mounted to and is in communication with a die-mounting pad 104 that is part of substrate 102. Col. 2, lines 63-64; Col. 3, lines 7-12; FIG. 2. A spacer 116 is mounted on the front surface 110 of the first semiconductor die 108, in electrical isolation from the die 108. Col. 3, lines 20-21, 45-46; FIG. 2. An end 130 of a wire 124 is bonded to the spacer 116. FIGs. 1 and 2. Although the other end of the wire 124 may be bonded to a bond pad 112 of the first semiconductor die or the die-mounting pad 104, Foster states that the purpose of bonding the wire to the spacer 116 is "not to make an electrical connection with the spacer," but "simply to hold the second end [130] of the wire [124] in place until a second die **140** is mounted on the spacer [116] . . ." Col. 4, lines 9-15; FIG. 2. Embedding the end 130 of the wire 124 in a layer of conductive material 146 that is the *same thickness as the bond*, that lies upon the surface of the spacer 116, and that

contacts the back surface 144 of the second die 140, "eliminates the need for an electrically conductive spacer 116 and a wire-bonding 'step' thereon." Col. 4, lines 49-54; FIG. 2. The conductive layer 146, connected to the wire 124 and the second semiconductor die 140, permits the second die 140 to be biased to the same or different electrical potential as the first die 108. Col. 4, lines 63-68.

(3) ANALYSIS

(a) FOSTER

Claims 18-21, 30, 31, 33-35 and 54 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in Foster.

It is respectfully submitted that the description of Foster does not anticipate each and every element of independent claim 18.

Independent claim 18 is directed to a semiconductor device assembly that includes a substrate, a first semiconductor device, a second semiconductor device, and spacers between the first and second semiconductor devices. The spacers, which protrude from a surface of the first semiconductor device, are "mutually laterally spaced" and "discrete" from one another. They communicate with a ground or reference voltage plane of the first semiconductor device, and with a back side of the second semiconductor device.

Each assembly described in Foster is limited to a single planar spacer 116/216 disposed between semiconductor dice 140 and 108. FIG. 2. Therefore, Foster does not expressly or inherently disclose mutually laterally spaced, discrete spacers, as required by independent claim 18.

Assuming, for argument's sake, that one skilled in the art would consider the adhesive layer 121/221 to be a spacer, which Applicant does not concede, Foster lacks any description that the adhesive layer 121/221 is laterally spaced from spacer 116/216.

For these reasons, it is respectfully submitted that the description of Foster does not anticipate each and every element of independent claim 18. As such, independent claims 18 is directed to subject matter that, under 35 U.S.C. § 102(b) is allowable over the disclosure of Foster.

Each of claims 19-21, 30, 31, 33-35, and 54 is allowable among other reasons, for depending directly or indirectly from independent claim 18, which is allowable.

Claim 33 is further allowable because Foster includes no express or inherent description of a semiconductor device assembly that includes three or more semiconductor devices.

Claim 54 is additionally allowable since Foster neither expressly nor inherently describes a semiconductor device assembly with at least one spacer that is secured to a contact pad of a semiconductor device. To the contrary, Foster explains that the spacer 116, 216 of a semiconductor device assembly may not be positioned over a bond pad 112 of a semiconductor device 108. Col. 3, lines 38-51. Instead, the spacers 116 and 216 are configured to have an outer periphery which is smaller than the inner periphery of a bond pad 112 arrangement of the semiconductor device 108 so that the spacers 116 and 216 may be located within the inner periphery of the bond pads 112 and, thus, do not cover the bond pads 112. *Id.*

Reversal of the 35 U.S.C. § 102(e) rejections of claims 18-21, 30, 31, 33-35, and 54 is respectfully requested, as is the allowance of each of these claims.

(B) REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 have been rejected under 35 U.S.C. § 103(a).

(1) LEGAL AUTHORITY

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) ART RELIED UPON

Pu

Pu teaches a stacked multi-chip structure. An adhesive layer 204a adheres a first die 206 to a substrate 202. Col. 4, lines 13-15; FIGs. 4A, 4B. Adhesive layer 204b adheres spacers 220 to the first die 206, and a second adhesive layer 204c adheres a second die 208 to the tops of the spacers 220. Col. 4, lines 17-20; FIGs. 4A, 4B. The spacers, which may be made of silicon or metal, provide sufficient rigidity to avoid compression (referred to in Pu as "the cushion effect") during the wire bonding process. Pu asserts that the cushion effect is a problem associated with other stacking methods that used compressible materials, such as polyimide tape. Col. 2,

lines 12-15; Col. 4, lines 36-39, 47-53; FIGs. 4A, 4B. The cushion effect occurs during wire bonding when a material compresses under the force applied to the material during the wire bonding process. As the material compresses, the wire that is to be bonded to the material no longer is in optimal contact with the surface of the material, resulting in a bond of substandard quality. Thus, Pu teaches away from the use of compressible spacers.

LoBianco

LoBianco teaches a multi-chip package in which two dice 14 and 16 are stacked and adhered together. A substrate 12 has a first die 14 adhered to the top surface thereof with an adhesive layer 13. Col. 3, lines 50-55; FIG. 3. Bond wires electrically connect bond pads of the die 14 to corresponding terminals of the substrate 12. A spacer 50, which may be made from a fiberglass matrix impregnated epoxy resin, ceramic, or plastic polymer (col. 7, lines 20-24), is placed atop the first die 14 with a layer of adhesive 54. Col. 6, lines 60-68; FIG. 8. An adhesive layer 40 is then dispensed onto the top of the first die 14 and around the spacer 50 and a second die 16 is pressed down onto the adhesive 40 until it contacts a layer of adhesive 52 on the top of the spacer 50. Col 7, lines 1-4; FIG. 8. The adhesive layers 40, 52, and 54 are cured and bonding pads on the second die 16 may be wire bonded to the substrate 12. Col. 5, lines 15-18; Col. 7, lines 34-36; FIGs. 3, 8. The spacer 50 and cured adhesive layers 40, 52, 54 provide support to the second die from the bending and shear forces imposed during the wire bonding process, forces that might otherwise fracture the die. Col. 5, lines 18-24; FIG. 2.

(3) ANALYSIS

(a) PU IN VIEW OF LOBIANCO

Claims 1, 3, 5-8, 10, 12-17, and 53 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over that taught in Pu, in view of teachings from LoBianco.

Independent claim 1 is directed to a semiconductor device assembly comprising at least one semiconductor device and at least one resiliently compressible spacer protruding from a surface of the at least one semiconductor device. The at least one resiliently compressible spacer defines a distance the surface of the at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

It is respectfully submitted that there are several reasons that the teachings of Pu and LoBianco do not support a *prima facie* case of obviousness against any of claims 1, 3, 5-8, 10, 12-17, or 53.

First, it is respectfully submitted that neither Pu nor LoBianco teaches or suggest all of the limitations of independent claim 1. Neither Pu nor LoBianco suggests a semiconductor device assembly that includes at least one resiliently compressible spacer. The spacer taught in Pu may be either silicon or metal. The spacers of LoBianco may be ceramic, epoxy, or a polymer. Therefore, neither of these references teaches or suggests a resiliently compressible spacer.

Second, as neither Pu nor LoBianco teaches or suggests a resiliently compressible spacer, neither of these references provides any suggestion or motivation to combine their teachings, nor would one of ordinary skill in the art be motivated to make the proposed combination. Instead, it

appears that, without the hindsight provided by the claims of the '258 Application, one of ordinary skill in the art wouldn't have been motivated to combine teachings from Pu and LoBianco in the asserted manner..

Third, Pu teaches away from the subject matter of independent claim 1. Pu teaches that compressible materials, such as polyimide tapes, are insufficiently rigid, resulting in a cushion effect on the second die, which negatively affects the quality and the reliability of the wire bonding. Pu, Col. 2, lines 12-14. Thus, Pu teaches away from a resiliently compressible spacer, which further indicates the non-obviousness of independent claim 1. *In re Hedges*, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986); M.P.E.P. § 2146(X)(D)(3)("proceeding contrary to accepted wisdom in the art is evidence of nonobviousness"); *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997); M.P.E.P. § 2144.05(III)("A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention.").

Fourth, it is respectfully submitted that Pu teaches away from the asserted combination of reference teachings. It has been asserted by the Office that one of ordinary skill in the art would have been motivated to replace the silicon or metal spacer 116 of Pu with a polyimide spacer 50 of LoBianco. It has been further asserted that a polyimide spacer 50 of the type taught in LoBianco would inherently be resiliently compressible. It is respectfully submitted that these assertions overlook that fact that the teachings of Pu are limited to semiconductor device assemblies that are configured to minimize the so-called "cushion effect," and that the use of a resiliently compressible spacer would not minimize but, rather, increase the "cushion effect." In

fact, Pu specifically teaches that "polyimide . . . causes the cushion effect . . ." Col. 2, lines 12-14.

Fifth, considering that Pu and LoBianco both teach the use of rigid, non-compressible materials to form spacers, it is respectfully submitted that one of ordinary skill in the art would have not reason to expect that teachings from Pu and LoBianco could be successfully combined to arrive at an assembly that includes at least one resiliently compressible spacer.

As a *prima facie* case of obviousness has not been established against any of claims 1, 3, 5-8, 10, 12-17, or 53, it is respectfully submitted that the subject matter to which each of these claims is directed is allowable under 35 U.S.C. § 103(a).

Claim 8 is additionally allowable because neither Pu nor LoBianco teaches or suggests a semiconductor device assembly that includes an adhesive material located between adjacent spacers.

Claim 17 is further allowable since Pu and LoBianco both lack any teaching or suggestion of a semiconductor device assembly that includes at least one resiliently compressible spacer secured to a noncircuit bond pad of a semiconductor device.

Claim 53 is also allowable since neither Pu nor LoBianco teaches or suggests a semiconductor device assembly that includes at least one resiliently compressible spacer secured to a contact pad of a semiconductor device.

(b) PU IN VIEW OF LOBIANCO AND FOSTER

Claims 11, 22, 18-23, 25, 28, 30-35, and 54 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Pu, in view of teachings from LoBianco and, further, in view of the subject matter taught in Foster.

Claims 11 and 12 are both allowable, among other reasons, for depending indirectly and directly, respectively, from independent claim 1, which is allowable.

As discussed above with respect to Pu and LoBianco, neither of these references provides any suggestion or motivation to combine their teachings in the asserted manner, nor would one skilled in the art be motivated to do so. Furthermore, it is respectfully submitted that Foster, which teaches assemblies that includes spacers 116 that may be formed from rigid materials, such as copper, silicon, Alloy 42, a ceramic, silicon dioxide, or a composite material (col. 3, lines 22-33), does not provide any teaching or suggestion that counters the facts that Pu teaches away from the combination of its teachings with those of LoBianco, that Pu teaches away from the subject matter recited in claims 11, 22, 18-23, 25, 28, 30-35, and 54, and that one of ordinary skill in the art ordinary skill wouldn't have been motivated to combine the teachings of Pu with those of LoBianco in the manner that has been asserted or have had any reason to expect that such a combination would successfully result in the claimed assemblies.

Therefore, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 11, 12, 18-23, 25, 30-35, or 54, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

(c) FOSTER IN VIEW OF LOBIANCO

Claims 1, 3, 5-8, and 10-16 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Foster, in view of the subject matter taught in LoBianco.

As discussed above, neither LoBianco nor Foster teaches or suggests a semiconductor device assembly that includes a resiliently compressible spacer, as would be required for the combined teachings of LoBianco and Foster to teach or suggest each and every element of independent claim 1. As such, it is respectfully submitted that, without the benefit of hindsight that the rejected claims provide to the Examiner, one or ordinary skill in the art wouldn't have been motivated to combine the teachings of Foster and LoBianco in the manner that has been asserted or had any reason to expect that the purported combination of reference teachings would have been successful. Therefore, LoBianco and Foster do not meet any of the criteria set forth in M.P.E.P. § 706.02(j) that would be necessary to establish a *prima facie* case of obviousness against claims 1, 3, 5-8, and 10-16.

It is respectfully that the 35 U.S.C. § 103(a) rejections of claims 1, 3, 5-8, 10-23, 25, 28, 30-35, 53, and 54 be reversed, and that each of these claims be allowed.

(C) ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claim 1 remains generic to both of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of this claim, claims 9, 24, and 29,

which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

(8) CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

(9) EVIDENCE APPENDIX

There is no EVIDENCE APPENDIX to this APPEAL BRIEF.

(10) RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a RELATED PROCEEDINGS APPENDIX.

(11) CONCLUSION

It is respectfully submitted that:

(A) Claims 18-21, 30, 31, 33-35 and 54 are allowable under 35 U.S.C. § 102(b) for reciting subject matter which is patentable over that described in Mandelman;

(B) Claims 1, 3, 5-8, 10, 12-17, and 53 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over the subject matter taught in Pu, in view of teachings from LoBianco;

(C) Claims 11, 22, 18-23, 25, 28, 30-35, and 54 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over the subject matter taught in Pu, in view of teachings from LoBianco and, further, in view of subject matter taught in Foster; and

(D) Claims 1, 3, 5-8, and 10-16 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over the subject matter taught in Foster, in view of the teachings of LoBianco;

Accordingly, it is respectfully requested that the rejections of claims 1, 3-8, 10-23, 25, 28, 30-35, 53, and 54 be reversed and that each of claims 1, 3-25, 28-35, 53, and 54 be allowed.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: October 23, 2006
BGP:JPN/eg
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CLAIMS APPENDIX

1. A semiconductor device assembly, comprising:

at least one semiconductor device; and

at least one resiliently compressible spacer protruding from a surface of the at least one semiconductor device, the at least one resiliently compressible spacer defining a distance the surface of the at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

3. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer protrudes from an active surface of the at least one semiconductor device.

5. The semiconductor device assembly of claim 4, comprising a plurality of spacers that are arranged to stably support the another semiconductor device.

6. The semiconductor device assembly of claim 1, further comprising:

the another semiconductor device positioned adjacent the at least one resiliently compressible spacer, opposite from the at least one semiconductor device.

7. The semiconductor device assembly of claim 6, further comprising:

adhesive material between the at least one semiconductor device and the another semiconductor device.

8. The semiconductor device assembly of claim 7, wherein the adhesive material is located between adjacent spacers.

9. The semiconductor device assembly of claim 6, wherein the at least one resiliently compressible spacer is electrically isolated from internal circuitry of the at least one semiconductor device.

10. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer comprises electrically conductive material.

11. The semiconductor device assembly of claim 10, wherein the at least one resiliently compressible spacer communicates with a ground plane of the at least one semiconductor device.

12. The semiconductor device assembly of claim 1, further comprising:

a substrate with which at least one semiconductor device is associated.

13. The semiconductor device assembly of claim 12, wherein the substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

14. The semiconductor device assembly of claim 12, wherein at least one bond pad of the at least one semiconductor device is in communication with a corresponding contact area of the substrate.

15. The semiconductor device assembly of claim 14, further comprising:

at least one discrete conductive element extending from the at least one bond pad, over an active surface of the at least one semiconductor device, to the corresponding contact area.

16. The semiconductor device assembly of claim 15, wherein heights of the at least one resiliently compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

17. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer is secured to noncircuit bond pads of the at least one semiconductor device.

18. A semiconductor device assembly, comprising:

a substrate;

a first semiconductor device associated with the substrate, bond pads of the first semiconductor device in communication with corresponding contact areas of the substrate;

mutually laterally spaced discrete spacers positioned on and protruding from an active surface of the first semiconductor device, at least one spacer of the mutually laterally discrete spacers being in communication with a ground or reference voltage plane of the first semiconductor device; and

a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane.

19. The semiconductor device assembly of claim 18, wherein the substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

20. The semiconductor device assembly of claim 18, wherein the bond pads and the corresponding contact areas communicate by way of discrete conductive elements positioned therebetween.

21. The semiconductor device assembly of claim 20, wherein the discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

22. The semiconductor device of claim 18, wherein the mutually laterally spaced discrete spacers are secured to noncircuit bond pads of the first semiconductor device.

23. The semiconductor device assembly of claim 22, wherein the mutually laterally spaced discrete spacers comprise conductive material.

24. The semiconductor device assembly of claim 23, wherein the mutually laterally spaced discrete spacers are electrically isolated from internal circuitry of the first semiconductor device.

25. The semiconductor device assembly of claim 23, wherein the mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of the first semiconductor device.

28. The semiconductor device assembly of claim 18, wherein at least one of the mutually laterally spaced discrete spacers is compressible.

29. The semiconductor device assembly of claim 18, wherein the second semiconductor device comprises a dielectric layer on at least portions thereof that contact the mutually laterally spaced discrete spacers.

30. The semiconductor device assembly of claim 18, wherein bond pads of the second semiconductor device communicate with the corresponding contact areas of the substrate by way of discrete conductive elements positioned therebetween.

31. The semiconductor device assembly of claim 18, further comprising:

an adhesive layer between the first semiconductor device and the second semiconductor device.

32. The semiconductor device assembly of claim 31, wherein at least some of the mutually laterally spaced discrete spacers extend through the adhesive layer.

33. The semiconductor device assembly of claim 18, further comprising:

at least one additional semiconductor device positioned over the second semiconductor device.

34. The semiconductor device assembly of claim 18, further comprising:

an encapsulant material substantially covering the first semiconductor device, the second semiconductor device, discrete conductive elements, and portions of the substrate located adjacent to the first semiconductor device.

35. The semiconductor device assembly of claim 18, further comprising:

at least one external connective element carried by the substrate and in electrical communication with at least one corresponding contact area of the substrate.

53. The semiconductor device assembly of claim 1, wherein the at least one resiliently compressible spacer is secured to a contact pad of the at least one semiconductor device.

54. The semiconductor device assembly of claim 18, wherein the at least one spacer is secured to a contact pad of at least one of the first semiconductor device and the second semiconductor device.